CLAIMS:

1. A module (102) for transmitting sets of data bits to another module via a communication bus (104), the module (102) comprising:

- bus invert coding means (106, 108, 112, 114, 116) for reducing the number of transitions on the communication bus (104) as the module (102) operates; the bus invert coding means (106, 108, 112, 114, 116) being adapted to:

- compare a set of data bits with a preceding set of data bits to determine an indication of the number of transitions required to transmit the set of data bits;

- invert the set of data bits prior to transmission if it is determined that the number of transitions required to transmit the set of data bits is greater than half the total number of bits in the set of data bits; and

- provide an indication of whether the set of data bits has been inverted;

- means adapted to generate respective copies of the data bits in the set of data bits; and

- means adapted to transmit to the other module, via the communication bus, the set of data bits, their respective copies and the indication of whether the set of data bits has been inverted.

2. A module as claimed in claim 1, wherein the means (110) adapted to generate respective copies of the data bits is further adapted to invert the respective copies.

3. A module as claimed in claim 1 or 2, further comprising:

- means (124) adapted to generate a first parity bit from the set of data bits;

wherein the means adapted to transmit is further adapted to transmit the first parity bit to the other module.

4. A module as claimed in claim 3, wherein the means (124) adapted to generate a first parity bit comprises one or more logic gates.

5. A module as claimed in claim 3 or 4, further comprising:

- means adapted to generate a copy of the first parity bit;

wherein the means adapted to transmit is further adapted to transmit the copy of the first parity bit to the other module.

6. A module as claimed in claim 5 when dependent on claim 2, wherein the means (126) adapted to generate a copy of the first parity bit is further adapted to invert the copy of the first parity bit.

7. A module as claimed in claim 5 or 6, wherein the indication of whether the set of data bits has been inverted is encoded in the first parity bit and its respective copy.

8. A module as claimed in claim 7, wherein the first parity bit and its respective copy are inverted before transmission if the set of data bits has been inverted by the bus invert coding means (106, 108, 112, 114, 116).

9. A module as claimed in claim 7, wherein the first parity bit and its respective copy are inverted before transmission if the set of data bits has not been inverted by the bus invert coding means (106, 108, 112, 114, 116).

10. A module as claimed in any preceding claim, wherein the bus invert coding means (106, 108, 112, 114, 116) comprises one or more logic gates.

11. A module as claimed in one of claims 1 to 6, wherein the indication comprises an invert signal.

12. A module as claimed in claim 11, further comprising:

- means adapted to generate a copy of the invert signal;

wherein the means adapted to transmit is further adapted to transmit the copy of the invert signal to the other module.

13. A module as claimed in claim 12, wherein the means (120) adapted to generate a copy of the invert signal is further adapted to invert the copy of the invert signal.

14.A module (128) for receiving sets of data bits from another module via a communication bus (104), the module (128) comprising:

- means adapted to receive a set of data bits, respective copies of the set of data bits and an indication of whether the set of data bits has been inverted;
- means (130) adapted to select the received data bits as the output of the module in the event that the indication of whether the set of data bits has been inverted indicates that the set of data bits has not been inverted, and to select the inverse of the received data bits as the output of the module in the event that the indication indicates that the set of data bits has been inverted.

15. A module as claimed in claim 14, wherein the respective copies of the set of data bits are inverted copies of the set of data bits.

16. A module as claimed in claim 14 or 15, further comprising means (64, 66) for detecting the presence of one or more errors in the received set of data bits.

17. A module as claimed in claim 16, wherein the means adapted to receive is further adapted to receive a first parity bit from the other module; and wherein the module (128) further comprises:

- means (64) adapted to generate a second parity bit from the received set of data bits; and

wherein the means (64, 66) adapted to detect the presence of one or more errors in the received set of data bits is adapted to compare the first and second parity bits.

18. A module as claimed in claim 17, wherein the means (64) adapted to generate a second parity bit comprises one or more logic gates.

19. A module as claimed in claim 16, 17 or 18, wherein the means (64, 66) adapted to detect the presence of one or more errors in the received data bits comprises a logic gate.

20. A module as claimed in one of claims 16 to 19, wherein the module (128) further comprises means for correcting errors in the received set of data bits, the means for

correcting errors being adapted to output a received data bit or its respective copy in response to a control signal output by the means (64, 66) adapted to detect.

21. A module as claimed in one of claims 17, 18 or 19, wherein the means adapted to receive is further adapted to receive a copy of the first parity bit from the other module.

22. A module as claimed in claim 21, wherein the indication of whether the set of data bits has been inverted is encoded in the received first parity bit and its copy.

23. A module as claimed in claim 22, wherein the module further comprises:

- means (140) adapted to generate a third parity bit from the respective copies of the set of data bits;
- means (66, 144, 146) adapted to compare the received first parity bit, the received copy of the first parity bit, the second parity bit and the third parity bit to determine whether the set of data bits has been inverted.

24. A module as claimed in one of claims 14 to 21, wherein the indication comprises an invert signal.

25. A module as claimed in claim 24, wherein the means adapted to receive is further adapted to receive a copy of the invert signal from the other module.

26. A module as claimed in claim 25, wherein the copy of the invert signal is an inverted copy of the invert signal.

27. A module as claimed in claim 25 or 26, further comprising means for detecting the presence of an error in the received invert signal or its respective copy.

28. A module as claimed in claim 27, wherein the means for detecting the presence of an error in the received invert signal or its respective copy compares the received invert signal and its respective copy.

29. A system comprising a module for transmitting (102) as claimed in one of claims 1 to 13 and a module for receiving (128) as claimed in one of claims 14 to 28, the modules being connected via a communication bus (104).